REMARKS

This responds to the Office Action mailed on December 13, 2004.

Claims 11, 15, 18, 22, 25, 35 and 41 are amended, no claims are canceled, and no claims are added; as a result, claims 11-25, 35-39, and 41-43 are now pending in this application.

§112 Rejection of the Claims

Claims 11-25, 35-39, and 41-43 were rejected under 35 U.S.C. § 112, second paragraph, for indefiniteness.

Each of the independent claims 11, 15, 18, 22, 25, 35 and 41 has been amended to more clearly define the invention and to eliminate the indefinite elements identified by the Examiner. Applicant submits that no new matter has been added since each of the additions is supported by the specification.

For example, the fifth paragraph in the DETAILED DESCRIPTION OF THE INVENTION states as follows. "Referring now to the drawings, FIG. 2 illustrates a top plan view of an integrated circuit die after it has been cut or sawed from a silicon wafer. FIG. 3 illustrates the integrated circuit die after undergoing the additional manufacturing process steps of the invention."

The amendments to the claims are further supported by the tenth paragraph. "FIG. 3 illustrates integrated circuit die 10 after undergoing the additional steps of the invention. The layer of remaining scribe 22 as it was prior to reduction is illustrated in phantom view in FIG. 3 (and also in FIG. 6 which is discussed below). The invention involves further removing the layer of remaining scribe 22 on the die and also increasing the smoothness and flatness of the perimeter edges 18 of a die. After separating a wafer into a plurality of dies, each die is further ground or polished by the process of the invention to remove a substantial amount of the remaining scribe 22 and reduce or eliminate any irregularities 24 in the edges 18. Thus, a die which has a smaller length and width and which has much smoother and flatter edges is produced."

§103 Rejection of the Claims

Claims 11-16, 18-25, 35-38, and 41-43 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Boruta (EP 06478904A1) in view of Camasta (U.S. Patent No. 3,545,325), Baker et al. (U.S. Patent No. 3,689,803) and Weisshaus et al. (Dicing article).

The Office Action takes the position that it would have been obvious to one of ordinary skill in the art at the time of the claimed invention to include a width of buffer area around active circuitry of die in Boruta, motivated by a desire to avoid damage to active circuitry from an edge defect as known in the art per Baker et al. with Baker et al. explaining that the width of the buffer area is dependent on the edge defect severity for a given dicing process.

The Office Action admits that Boruta does not disclose that side surfaces of diced die that are ground or polished "surfaces" without substantially any irregularities that produce weak points in the substrate." The Office Action then cites Camasta as disclosing a dicing apparatus that inherently results in a "ground" side surface from the grinding action of the blade (i.e. as disclosed in Weisshaus et al.). Furthermore, the Office Action posits that the dicing apparatus of Camasta "is capable of cutting chip devices from a wafer so that the chip devices have substantially smooth edge surfaces and uniform dimensions," wherein the dicing apparatus "substantially eliminates the rough edges, broken corners..."

The Office Action further concludes that it would have been obvious to one of ordinary skill in the art at the time of the claimed invention to adopt the dicing apparatus of Camasta for practicing the dicing method of Boruta. The Office Action apparently takes the position that one of ordinary skill in the art would have been motivated to adopt the dicing apparatus of Camasta for practicing the method of Boruta because the apparatus "substantially eliminates" undesirable imperfections that "could affect the operation of subsequent handling operations of the chip devices".

Each of the independent claims 11, 15, 18, 22, 25, 35 and 41 has been amended to set forth that, for example in claim 11, each planar perimeter side surface of the semiconductor die has an initial size, after the die is initially cut, that is reduced to a final size, after the die is further ground or polished to eliminate irregularities that produce weak points in the substrate, the final size being smaller than the initial size. Not only is the top working surface smaller from

grinding the sides, but the surface area of an adjacent side is also smaller because the ends of a side are shortened (where the two sides meet) due to the polishing.

Thus, with these amendments to the independent claims and with the above explanation given above, no combination of the cited prior art would render obvious the amended independent claims. For example, none of the cited prior references disclose that the final size is smaller than the initial size. Therefore, the Examiner is respectfully requested to reconsider this rejection of the claims.

Since the dependent claims include all the limitations of the independent claim, upon which they depend, the dependent claims are also not anticipated by the cited prior art. The dependent claims are believed allowable for the same reasons as the related independent claim, as well as their own additional characterization.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney, John Garrett, at (847) 508-2371 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

AARON M. SCHOENFELD

By his Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(847) 508-2371

Date _____

By _____
John R. Garrett
Reg. No. 27,888

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 14 day of February, 2005.

Tina Kohut
Name

Signature